UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,611	03/31/2000	Carl M. Ellison	042390.P8112	2172

			EXAMINER
8791	7590	02/11/2004	TRAN, ELLEN C

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15

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>31 March 2000</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-60</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-60</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

    a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

NORMAN M. WRIGHT
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>7-12</u>.

4) ☐ Interview Summary (PTO-413)

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

Detailed Action

1.   This action is responsive to communication: original application filed

31 March 2000.

2.   Claims 1-60 are currently pending in this application. Claims 1, 16, 31, and 46

are independent claims.

Double Patenting

3.   The nonstatutory double patenting rejection is based on a judicially created

doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the

unjustified or improper timewise extension of the "right to exclude" granted by a patent

and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11

F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225

USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA

1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*,

418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to

overcome an actual or provisional rejection based on a nonstatutory double patenting

ground provided the conflicting application or patent is shown to be commonly owned

with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal

disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37

CFR 3.73(b).

4.   **Claims 1-12, 16-27, 31-42, and 46-57** are rejected under the judicially created

doctrine of obviousness-type double patenting as being unpatentable over claims 1-44

of U.S. Patent No. 6,633,963 B1 (hereinafter '963) by Ellison et al. Although the

conflicting claims are not identical, they are not patentably distinct from each other

because the wording reflexes the same limitation.

> **As to independent claim 16, "A method comprising: configuring an access**
>
> **transaction generated by a processor ... access information"** is taught in '963
>
> claim 12.

> -   **Specifically "by a configuration storage containing configuration**
>
> **parameters, the processor having a normal execution mode and an isolated**
>
> **execution mode"** has the same intensive use as "having a normal execution mode and
>
> an isolated execution mode using a configuration storage storing configuration settings"

> -   **"the access transaction having access information"** has the same
>
> intensive use as "the access transaction includes access information"

> -   **"checking the access transaction by an access checking circuit using at**
>
> **least one of the configuration parameters and the access information"** has the
>
> same intensive use as "checking the access transaction by a multi-memory zone
>
> access checking circuit using at least one of the configuration settings and the access
>
> information; and generating an access grant signal if the access transaction is valid".

> **As to dependent claim 17, "wherein the configuration parameters include**
>
> **an isolated setting and an execution mode word"** is taught in '963 claim 12 col. 17,
>
> lines 33-39 "having a normal execution mode and an isolated execution mode using a

configuration storage storing configuration settings, the configuration storage including

a process control register storing an execution mode word that is asserted as an

execution mode signal when the processor is configured in the isolated execution

mode".

As to dependent claim 18, "wherein the access information comprises a

physical address"" is taught in '963 claim 12 col. 17 lines 45-46 "wherein the access

transaction includes access information including a physical address";

"and an access type, the access type indicating if the access transaction is one

of a memory access, an input/output access, and a logical processor access, the

physical address being one of a translation lookaside buffer (TLB) physical address

from a TLB and a front side bus (FSB) physical address from an FSB" is shown in '963

claim 12 col. 17, lines 35-46 "the configuration storage including a process control

register storing an execution mode word that is asserted as an execution mode signal

when the processor is configured in the isolated execution mode, the configuration

settings including a plurality of subsystem memory range settings, a memory base

value, and a memory length value, a combination of at least the base and length

values to define an isolated memory area in a memory external to the processor that is

accessible to the processor in the isolated execution mode, wherein the access

transaction includes access information including a physical address".

As to dependent claim 19, "wherein configuring the access transaction

comprises: defining an isolated memory area corresponding to a memory

external to the processor by the isolated setting contained in a setting storage"

has the same intensive use as '963 claim 13 "wherein each subsystem memory range
setting corresponds to a memory zone for a subsystem in an isolated memory area in a
memory external to the processor".

As to dependent claim 20, "wherein defining the isolated memory area
comprises: forming the isolated setting by a combination of at least two of a
base value, a mask value, and a length value stored in a base register, a mask
register, and a length register, respectively" is shown in '963 claim 12 col. 17 lines
39-45 "the configuration settings including a plurality of subsystem memory range
settings, a memory base value, and a memory length value, a combination of at least
the base and length values to define an isolated memory area in a memory external to
the processor that is accessible to the processor in the isolated execution mode".

As to dependent claim 21, "wherein configuring the access transaction
further comprises: asserting the execution mode word stored in a processor
control register when the processor is configured in the isolated execution
mode" is disclosed in '963 claim 12 col. 17 lines 34-39 "using a configuration storage
storing configuration settings, the configuration storage including a process control
register storing an execution mode word that is asserted as an execution mode signal
when the processor is configured in the isolated execution mode".

As to dependent claim 22, "wherein checking the access transaction
comprises: detecting if the TLB and FSB physical addresses are within the
isolated memory area defined by the isolated setting by TLB and FSB address
detectors, respectively, the TLB and FSB address detectors generating

processor and FSB isolated acc ss signals, respectively" is taught in '963

claim 16 "wherein checking the access transaction comprises detecting if the physical

address is within a currently active subsystem's associated memory zone as defined

by the subsystem memory range setting for the subsystem by a subsystem address

detector, the subsystem address detector generating a subsystem address matching

signal".

As to dependent claim 23, "wherein checking the access transaction

further comprises: generating a processor snoop access signal by a snoop

checking circuit" is taught in claim 12 col. 17, lines 47-50 "checking the access

transaction by a multi-memory zone access checking circuit using at least one of the

configuration settings and the access information; and generating an access grant

signal".

As to dependent claim 24, "wherein generating the processor snoop

access signal comprises: combining a cache access signal, the FSB isolated

access signal, and an external isolated access signal from another processor by

a snoop combiner, the combined cache access signal, the processor isolated

access signal and the external isolated access signal corresponding to the

processor snoop access signal" is shown in '963 claim 17 "wherein generating an

access grant signal if the access transaction is valid comprises generating an access

grant signal by an access grant generator if both the subsystem address matching

signal and the execution mode word signal are asserted".

As to dependent claim 25, "wherein checking the access transaction further comprises: generating an access grant signal indicating if the access transaction is valid by an access grant generator" is disclosed in '963 claim 12, col. 17, lines 50-51 "and generating an access grant signal if the access transaction is valid".

As to dependent claim 26, "wherein the logical processor access is one of a logical processor entry and a logical processor exit" is taught in '963 claim 12 col. 17 lines 32-33 "configuring an access transaction generated by a processor having a normal execution mode" (i.e. "processor having normal execution mode" same as "logical entry" and "logical exit").

As to dependent claim 27, "wherein checking the access transaction comprises: managing a logical processor operation caused by the logical processor access by a logical processor manager" is shown in '963 claim 16 "wherein checking the access transaction comprises detecting if the physical address is within a currently active subsystem's associated memory zone as defined by the subsystem memory range setting for the subsystem by a subsystem address detector" (i.e. "managing" or "manager" same as "detecting" and "detector")

As to independent claims 1, this claim is the apparatus comprising the same method of claim 16 and is similarly rejected along the same rationale.

As to independent claim 31, this claim is a system comprising a chipset, which contains the same method as claim 16 and is similarly rejected along the same rationale.

As to independent claim 46, this claim is a computer program product

comprising the same method as claim 16 and is similarly rejected along the same

rationale.

As to dependent claims 2-12, 32-42, and 47-57 these claims incorporated

substantially similar subject matter as cited in claims 17-27 and are similarly rejected

along the same rationale.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

6.   **Claims 13-15, 28-30, 43-45 and 58-60** are rejected under 35 U.S.C. 103(a) as

being unpatentable over '963 as applied to claims 1-12, 16-27, 31-40 and 46-57 above

and in further view of Panwar et al. U.S. Patent No. 6,035,374 (hereinafter '374).

As to dependent claim 28, the following is not explicitly taught in '963 **"wherein**

managing the logical processor operation comprises: storing a logical processor

count indicating a number of logical processors currently enabled in a logical

processor register; enabling a logical processor state when the logical

processor access is valid by a logical processor state enabler updating the

logical processor count according to the logical processor access by a logical

processor updater, the logical processor updater being enabled by the enabled

logical processor state determining if the logical processor count is equal to a minimum logical processor value by a minimum detector; and determining if the logical processor count exceeds a maximum logical processor value by a maximum detector" however "ISU 206 (shown in greater detail in FIG. 8) is operative to schedule and dispatch instructions as soon as their dependencies have been satisfied into an appropriate execution unit (e.g., integer execution unit (IEU) 208, or floating point and graphics unit (FGU) 210). ISU 206 also maintains trap status of live instructions. ISU 206 may perform other functions such as maintaining the correct architectural state of processor 102, including state maintenance when out-of-order instruction processing is used. ISU 206 may include mechanisms to redirect execution appropriately when traps or interrupts occur and to ensure efficient execution of multiple threads where multiple threaded operation is used. Multiple thread operation means that processor 102 is running multiple substantially independent processes simultaneously ... state machines 301 are implemented in ISU 206 by maintaining virtual processor status information in ISU 206. Although other functional units use the thread ID to implement multiprocessors in accordance with the present invention, ISU 206 uses the virtual processor status information ... Hence, to ease circuit complexity and improve operation speed, it is advantageous to implement state machines 301 in ISU 206" is taught in '374 col 13, lines 9-35.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the access transactions generated by a processor with isolated and normal execution modes taught in '963 to include a method for counting processors

being utilized. One of ordinary skill in the art would have been motivated to perform

such a modification because the method of executing coded instruction in a

dynamically configurable multiprocessor is well known in the art see '374 (col. 4, lines

38 et seq.) "A processor in accordance with the present invention includes a processor

creation unit responsive to a processor create command to output signals indicating a

current processor configuration and plurality of virtual or logical processors each virtual

processor ...The state machines maintain processor status information representative

of whether the processor is available to receive and execute instructions. The

processor further includes status logic analyzing expected latency of instructions on

each processor and updating the state machine corresponding to any processor having

an instruction with an expected latency greater than a preselected threshold".

As to dependent claim 29, "wherein updating the logical processor count

comprises: initializing the logical processor register when there is no enabled

logical processor" is taught in '374 col 13, lines 9-35 "ISU 206 (shown in greater

detail in FIG. 8) is operative to schedule and dispatch instructions as soon as their

dependencies have been satisfied into an appropriate execution unit (e.g., integer

execution unit (IEU) 208, or floating point and graphics unit (FGU) 210). ISU 206 also

maintains trap status of live instructions ... Although other functional units use the

thread ID to implement multiprocessors in accordance with the present invention, ISU

206 uses the virtual processor status information to implement the active, nap, and

sleep states described hereinbefore. Hence, to ease circuit complexity and improve

operation speed, it is advantageous to implement state machines 301 in ISU 206".

As to dependent claim 30, "**wherein updating the logical processor count comprises: updating the logical processor count in a first direction when the access transaction corresponds to the logical processor entry; and updating the logical processor count in a second direction opposite to the first direction when the access transaction corresponds to the logical processor exit**" is taught in '374 col 13, lines 9-35 "ISU 206 (shown in greater detail in FIG. 8) is operative to schedule and dispatch instructions as soon as their dependencies have been satisfied into an appropriate execution unit (e.g., integer execution unit (IEU) 208, or floating point and graphics unit (FGU) 210). ISU 206 also maintains trap status of live instructions. ISU 206 may perform other functions such as maintaining the correct architectural state of processor 102, including state maintenance when out-of-order instruction processing is used. ISU 206 may include mechanisms to redirect execution appropriately when traps or interrupts occur and to ensure efficient execution of multiple threads where multiple threaded operation is used. Multiple thread operation means that processor 102 is running multiple substantially independent processes simultaneously".

As to dependent claims 13-15, 43-45, and 58-60 these claims incorporated substantially similar subject matter as cited in claims 28-30 and are similarly rejected along the same rationale.

Conclusion

7.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

     Barnett   U.S. Patent No. 6,292,874 issued dated: Sep. 18, 2001

     Browne   U.S. Patent No. 6,272,533 issued dated: Aug. 7, 2001

     Ellison et al. U.S. Patent No. 6,507,904 issued dated: Jan. 14, 2003

8.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Ellen C Tran whose telephone number is

(703) 305-8917. The examiner can normally be reached on 6:30 am to 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Gregory A Morse can be reached on (703) 308-4789. The fax phone

number for the organization where this application or proceeding is assigned is 703-

872-9306.

     Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is (703) 306-

5484.

Ellen. Tran
Patent Examiner
Technology Center 2134
February 6, 2004

NORMAN M. WRIGHT
PRIMARY EXAMINER